VLSI Design Tools & Technology (VDTT) Programme

Dated: 24.04.2019

Subject: Short-listing Criteria for admissions in 2019

The Programme Executive Committee (PEC) of the VDTT programme met on 18th and 24th April 2019. The agenda included the shortlisting of M. Tech (VDTT) and MS(R) applications.

1. **The following short listing criteria were decided for the M. Tech programme in VLSI Design Tools and Technology (JVL).**

i) Direct admission (Full time with GATE): Nil

ii) Call for interview (Full time with GATE):

GATE Discipline	Category	Minimum GATE Score	Eligibility Criteria
EC	GE/GE(EW)/OBC (NCL)	790	60% or 6 CGPA on 10 point scale
	SC/ST/PH	740	55% or 5.5 CGPA on 10 point scale
EE	GE/GE(EW)/OBC (NCL)	845	60% or 6 CGPA on 10 point scale
	SC/ST/PH	795	55% or 5.5 CGPA on 10 point scale
CS	GE/GE(EW)/OBC (NCL)	655	60% or 6 CGPA on 10 point scale
	SC/ST/PH	605	55% or 5.5 CGPA on 10 point scale
IN	GE/GE(EW)/OBC (NCL)	770	60% or 6 CGPA on 10 point scale
	SC/ST/PH	720	55% or 5.5 CGPA on 10 point scale
Others	GE/GE(EW)/OBC (NCL)	850	60% or 6 CGPA on 10 point scale
	SC/ST/PH	800	55% or 5.5 CGPA on 10 point scale
	B.Tech from IITs		CGPA ≥ 8 (GATE score not required)

NOTE:

A. B.Tech graduates from IITs are exempt from the requirement of a GATE score for the full time JVL programme.

B. If a candidate has applied for the programme, and if he/she meets the shortlisting criteria, he/she may appear for the interview even if he/she has not received a call letter. However, he/she needs to bring the original transcripts with him/her.

C. Sponsors eligible to sponsor a student should have entered into or committed to entering into a MoU with the VDTT Programme and should be willing to accept the terms and conditions stipulated, prior to the interview dates.

iii) **Call for interview for Full-Time sponsored, Part-Time Regular & Part-Time Industry sponsored candidates (Part-time):**

1. Candidates should be an employee of a sponsoring company with a confirmation of sponsorship from the sponsor required for being called for the interview. The sponsor should have entered into or committed to entering into a MoU with the VDTT Programme and should be willing to accept the terms and conditions stipulated, prior to the interview dates.
2. He/She should have a minimum of 1 year experience in research or development.
3. He/she should have a minimum 60% or 6 CGPA on a scale of 10 in the qualifying degree.

The candidates will be interviewed by the PEC on May 13th (Monday) 2019, followed by an interview of the shortlisted candidates with the sponsoring industries on May 14th (Tuesday) 2019.

(Prof. Jayadeva)
Coordinator, VDTT Programme

2. **The following short listing criteria were decided for the MS(R) <u>programme in VLSI Design Tools and Technology (JVY)</u>.**

i) Direct admission (Full time with GATE): Nil

ii) Call for interview (Full time with GATE):

GATE Discipline	Category	Minimum GATE Score	Eligibility Criteria
EC	GE/GE(EW)/OBC (NCL)	790	60% or 6 CGPA on 10 point scale
	SC/ST/PH	740	55% or 5.5 CGPA on 10 point scale
EE	GE/GE(EW)/OBC (NCL)	845	60% or 6 CGPA on 10 point scale
	SC/ST/PH	795	55% or 5.5 CGPA on 10 point scale
CS	GE/GE(EW)/OBC (NCL)	655	60% or 6 CGPA on 10 point scale
	SC/ST/PH	605	55% or 5.5 CGPA on 10 point scale
IN	GE/GE(EW)/OBC (NCL)	770	60% or 6 CGPA on 10 point scale
	SC/ST/PH	720	55% or 5.5 CGPA on 10 point scale
Others	GE/GE(EW)/OBC (NCL)	850	60% or 6 CGPA on 10 point scale
	SC/ST/PH	800	55% or 5.5 CGPA on 10 point scale
	B.Tech from Centrally Funded Technical Institutes (CFTIs)		CGPA ≥ 8 (GATE score not required)

NOTE:

A. Centrally Funded Technical Institutes are exempt from the requirement of a GATE score for the full time JVY programme.

B. If a candidate has applied for the programme, and if he/she meets the shortlisting criteria, he/she may appear for the interview even if he/she has not received a call letter. However, he/she needs to bring the original transcripts with him/her.

C. Sponsors eligible to sponsor a student should have entered into or committed to entering into a MoU with the VDTT Programme and should be willing to accept the terms and conditions stipulated, prior to the interview dates.

iii) **Call for interview for Full-Time sponsored, Part-Time Regular & Part-Time Industry sponsored candidates (Part-time):**

1. Candidates should be an employee of a sponsoring company with a confirmation of sponsorship from the sponsor required for being called for the interview. The sponsor should have entered into or committed to entering into a MoU with the VDTT Programme and should be willing to accept the terms and conditions stipulated, prior to the interview dates.
2. He/She should have a minimum of 1 year experience in research or development.
3. He/she should have a minimum 60% or 6 CGPA on a scale of 10 in the qualifying degree.

The candidates will be interviewed by the PEC on May 13th (Monday) 2019, followed by an interview of the shortlisted candidates with the sponsoring industries on May 14th (Tuesday) 2019.

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