Dear Applicant,

Thank you for your interest in the Inter-Disciplinary Master of Technology Program in VLSI Design Tools and Technology (VDTT). You are invited to appear for selection as per the following schedule:-

Interview dates: May 21st – 22nd, 2018

Time: 08:30 AM

Venue: VDTT Office, Block IV, Room No. 202

Candidates shortlisted in the interview/written test of 21st May will be interviewed on 22nd May by the sponsors. The interview/written test will be based on fundamentals, including analytical and quantitiative aptitude based questions, and questions on circuits, devices, systems, and basic programming skills.

This call for interview/written test is subject to your satisfying the eligibility and short-listing criteria for the above program are available at http://vdtt.iitd.ac.in.

- **If you have applied and meet the shortlisting criteria, but have not received a call letter, you may appear for the interviews with your original documents and a copy of your application.**
- **If you do not meet the shortlisting criteria, but have accidentally received a call letter, please immediately contact Mr. Rakesh at (011) 2659 6103.**
- We have also commenced a MS(Research) in VDTT in addition to the M.Tech (VDTT). The MS(R) programme is more focussed on project work, and all courses may be custom selected in consonance with the project, unlike the case of a M.Tech programme where core courses are mandatory and elective courses may be chosen from a list. The MS(R) thesis is intended to be more research oriented, in keeping with the trend in industry for an increasing research content in theses at the masters level.
- **Should you wish to opt for MS(R) instead of M.Tech even now, please let us know.** You may also write for any clarification in case you wish to examine the option.
- You may be aware that the programme has two new streams in addition to the traditional design one. The stream on Embedded Intelligent Systems was introduced to enable a focus on machine learning, intelligent systems, and embedded intelligence. The stream on micro and nano devices has a focus on nanotechnology and sensors.

1. Documents to be presented at the time of interview / written test:
   a. This letter
   b. Original degree and marks certificates of all qualifying examinations
   c. Score Card of GATE / CEED / Other National Level Examination (if applicable)
   d. OBC (Non-creamy Layer) / SC / ST / PH certificate (if applicable). (Please see http://www.ncbc.nic.in for details about OBC and Non-creamy layer)
   e. Sponsorship / No-objection Certificate (for Part-Time / Sponsored Candidates) (exactly in the wordings as given in the information brochure on the PG admission website, page 8)
   Note: Attested copies of all above original documents
2. Academic documents to be presented at the time of interview / written test:
   Your Bachelors' and /or Masters' project dissertation
3. A list of provisionally selected candidates will be displayed on the date of interviews after all the interviews are over, on the VDTT notice board on May 22, and subsequently on the website http://vdtt.iitd.ac.in. In the event of unforeseen delays, the list may be displayed on the morning of the 23rd of May. No candidate would be intimated by post or other modes of communication. If selected, you would be given a week's time to deposit the fees. The details of fees payable can be found on the information brochure on the PG admission website.

4. Candidates coming for the interview/written test would be provided accommodation in the student hostels on sharing basis on payment of Rs. 400 per day for boarding and lodging. No bedding would be available and candidates are required to make their own arrangement for bedding. Male students would be accommodated in Satpura (Phone no. 011-2659 7066, 2659 6617) and Female students in Kailash (Phone no. 011-2659 6839, 2659 6826) on production of a Demand draft for the amount drawn in favour of "Dean's Discretionary Fund, <Hostel Name> hostel". Please note that the temperatures in Delhi in the month of April-July would be in the range of 40-45 ^{o}C.

5. For any clarifications, please call 011-2659-6103 or e-mail: vdttoffice@gmail.com with subject line "Regarding Master of Technology in VLSI DESIGN TOOLS AND TECHNOLOGY(JVL) admissions"

VDTT Programme Co-ordinator