VLSI Design Tools & Technology (VDTT) Programme

The following short listing criteria were decided over and above the minimum eligibility condition as laid out in the prospectus.

ii) Call for interview (Full time with GATE):

GATE Discipline	Category	Minimum GATE Score	Minimum degree performance
EC	GE	800	60% or 6.75 on 10 point scale
	SC/ST/PH	750	55% or 6.25 on 10 point scale
EE	GE	800	60% or 6.75 on 10 point scale
	SC/ST/PH	750	55% or 6.25 on 10 point scale
CS	GE	730	60% or 6.75 on 10 point scale
	SC/ST/PH	680	55% or 6.25 on 10 point scale
IN	GE	750	60% or 6.75 on 10 point scale
	SC/ST/PH	700	55% or 6.25on 10 point scale
Others	GE	850	60% or 6.75 on 10 point scale
	SC/ST/PH	800	55% or 6.25 on 10 point scale
IIT B.Tech.	-		CGPA >= 8 GATE score not required)

NOTE:

A. Centrally Funded Technical Institutes other than the IITs are not exempt from the requirement of a GATE score for the full time programme.

B. If you have applied to the programme, and if you meet the shortlisting criteria you may appear for the interview even if you have not received a call letter. However, please bring your transcripts with you.

ii) **Call for interview for Full-Time sponsored, Part-Time Regular & Part-Time Industry sponsored candidates (Part-time)**

A **Candidates should be an employee of a sponsoring company with a confirmation of sponsorship from the sponsor required for being called for the interview.**

B **He/She should have a minimum of 1 year experience in research or development.**

C **He/she should have a minimum 70% or 7.75 on a scale of 10 in the qualifying degree.**

The candidates will be interviewed by the PEC on May 15th (Monday) 2017, followed by an interview of the shortlisted candidates with the sponsoring industries on May 16th (Tuesday) 2017.